What is claimed is:

1. An overlay target comprising:

first and second test patterns, each including an upper grating layer and a lower grating layer, each grating layer including a series of substantially parallel lines, the upper grating lines of each test pattern aligned to be substantially parallel to the lower grating lines of the same test pattern, each test pattern having an associated offset bias defined by the lateral offset of the upper and lower grating layers of the test pattern, where a single line pitch is used for all gratings in all test patterns and where the difference between the offset bias of the first test pattern and the offset bias of the second test pattern is substantially equal to the line pitch divided by four.

2. An overlay target as recited in claim 1, wherein the magnitude of the offset bias of the first test pattern is equal to the line pitch divided by eight

3. An overlay target as recited in claim 1, wherein the upper and lower grating lines of the first test pattern are substantially parallel to the upper and lower grating lines of the second test pattern.

4. An overlay target as recited in claim 1, that further comprises:

a third test pattern, including an upper grating layer and a lower grating layer, each grating layer including a series of substantially parallel lines, the lines of the upper and lower gratings of the third test pattern aligned to be substantially parallel to each other, where the lines in the third test pattern are spaced at the same line pitch used for the first and second test patterns.

5. An overlay target as recited in claim 4, where the grating lines of the first, second and third test patterns have three different angular orientations in the plane of the wafer.

6. A method for optically inspecting and evaluating a semiconductor wafer, the method comprising:

identifying a group of semiconductor wafer parameters to be evaluated;

providing more than one test patterns on the wafer such that the test patterns have some common physical properties and at least one physical property has different values at, at least two test patterns;

providing a theoretical model for the optical response of each test pattern where the model has adjustable unknown parameters;

measuring optical responses of the said test patterns;

assigning initial estimates to the unknown parameters;

applying an iterative search including the steps of:

calculating the optical responses of the said test patterns using the said theoretical models, based on the current estimates of the parameters;

comparing the sets of calculated and measured optical responses of said test patterns; and

updating the estimate of the unknown parameters in a way to minimize a norm of the difference between the measured and calculated optical responses of all test patterns.

7. A method as recited in claim 6, wherein the step of measuring includes measuring adjacent multiple test patterns.

8. A method as recited in claim 6, wherein the step of measuring includes measuring sites at multiple dies of a wafer or sites otherwise distributed over a wafer.

9. A method as recited in claim 6, wherein the step of measuring includes measuring multiple wafers.

10. A method as recited in claim 6, wherein said iterative search method is a genetic algorithm.

11 A method as recited in claim 6, wherein said iterative search method is a simulated annealing algorithm.

12 A method as recited in claim 6, wherein said iterative search method is the Levenberg-Marquardt algorithm.

13 A method as recited in claim 6, at least one of the semiconductor wafer parameters is selected from a group consisting of: line width, line spacing, line sidewall profile and overlay.